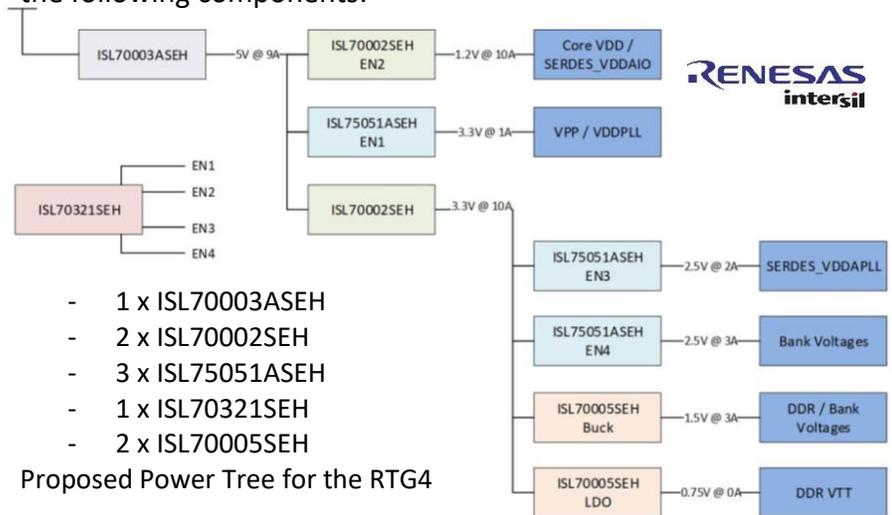


Matching Components for your RTG4 Design

1. Power your RTG4 with a full Intersil / Renesas solution

Intersil is developing a RTG4 Power reference Design that uses the following components:



Please be aware that at a later stage (Q1/2020) all the necessary files will be available from Intersil / Renesas for example BOM, Gerberfiles and a AppNote.

2. Optical Transceivers for RTG4 SerDes from Reflex Photonics

Reflex Photonics Demonstrated the possibility to use their Optical Transceiver directly connected to the RTG4 SerDes 3.125Gbps in October 2019 at the MicroChip Space Forum. The Reflex Photonics Modules are available as Transceivers with 4TRx channels in a very small package 20 x 14 x 5mm where no soldering is needed (Interposer).



If more channels are needed Reflex also offers 12Rx or 12Tx Modules. These optical Transceivers are used more and more in Traditional Space applications as well as in New Space Constellation Applications. Reflex offers very competitive pricing compared to traditional copper based data transfer solutions. In addition to that the optical data transfer offers much more advantages for your design. Your harness will be much lighter and smaller in diameter, lower power, electrical isolation, very high data transfer rate in a very small PCB area and more....

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3. Find the right Clocks for your RTG4 Design

Q-Tech offers Oscillators for the RTG4 MicroChip / Microsemi FPGAs Where the recommended parts are 2.5V LVDS, 3.3V CMOS, and 2.5V CMOS. All of these types can be found in the Q-Tech portfolio. See below Links to the relevant datasheets at Q-Tech.



- Class B+ Types → <https://q-tech.com/2016/07/new-b-space-oscillators-featuring-4pt-mount-high-shock-designs/>
- Multi-Output LVDS → <https://q-tech.com/2019/08/press-release-space-multiple-output-lvds-oscillator/>
- QT626L CMOS XOs → <https://q-tech.com/wp-content/uploads/QPDS-0118-QT625L.pdf>

4. SpW IP for your RT4 Design from 4Links

4Links' SpaceWire IP is based on a version of the CoDec (Coder / Decoder) used in its test equipment for SpaceWire. And the best part of it is it is for free.

Thousands of SpaceWire ports of this test equipment have proved to be interoperable with all the SpaceWire designs to which they have been connected. **The IP is free and flight proven** as the fundamental interconnect on a satellite. It also complements the test solutions and cabling on offer by 4Links.

The IP is implemented in VHDL, but is designed to be instantiated in Verilog with minimal effort. The IP is Supplied as a complete package:

- Standard, easy to use FIFO-style interface to user logic (Data Flow Channel, DFC)
- HDL simulation test bench
- Traffic generator
- Traffic logger (logging all the received traffic)



The simulation test bench (picture on the right) enables you to easily see how the IP operates and how to integrate it into your design. A traffic generator and logger are included in the test-bench connecting to the 4Links standard Data Flow Channels (used to connect to all 4Links IP). The generator and logger use a simple text based file allowing easy modification and checking of the vectors, so you can customise it to model the actual data in the design.

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